ABSTRACT

A method and system for co-verifying a hardware simulation of a field-programmable-system-level integrated circuit (FPSLIC) and a software simulation of the field-programmable-system-level integrated circuit. A FPSLIC device is simulated in hardware, and a simulator-port layout of the FPSLIC device is generated. In software, the method separately simulates, with an instruction-set simulator, the FPSLIC device, and outputs register contents from the instruction-set software. The contents from the simulator-port layout are verified with the register contents. Additionally, the method may further include outputting peripheral contents from the instruction-set simulator, and verifying contents from the simulator-port layout with the peripheral contents. UART contents also may be outputted from the instruction-set simulator, and verified with contents from the simulator-port layout with the UART contents.

T:\ATML\ATML03US.AP-11/1/98

LAW OFFICES
DAVID NEWMAN
CHARTERED
CENTENNIAL SQUARE
P.O. BOX 2728
LA PLATA, MD 20646
(301) 934-6100